Changes to IEC 62386 enabling DALI-2 certification

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This DALI Alliance Technical Note describes the key changes introduced by the major revision of IEC 62386 in 2014, which in turn enabled the DALI-2 certification program.

1. Overview

The DALI protocol was first drafted in the late 1990s. DALI is specified in the international standard IEC 62386. Both the DALI protocol and IEC 62386 have undergone a number of revisions as they have evolved.

A major revision of IEC 62386 took place in 2014. The changes were designed to improve interoperability and fill the gaps in the original standard. The revised standard added new features, and introduced standardisation of control devices, while maintaining backwards compatibility.

The revisions to IEC 62386 later enabled the development and launch of the DALI-2 certification program.

2. Improvements and additions

2.1 Parts 101 & 102 restructured

There were many improvements in the new version of the standard, including several new commands and features. Also, for the first time, IEC 62386 included standardisation of control devices.

To accommodate this, changes were necessary in Parts 101 and 102 to ensure there would be a clean split between system requirements in Part 101 and control-gear requirements in Part 102. The Tables below list some of the most important changes in Parts 101 and 102.

Revision of Part 101: General requirements - System

- Bus timing requirements are now collected together (from Part 102 and a previous draft of Part 103), allowing for control devices, including single-masters and multi- masters
- Insulation and earthing requirements are changed/added
- Operation through power interruptions is now defined, including short interruptions and long interruptions
- Bus power supplies and advanced bus power supplies have defined start-up timing
- Signal voltage rating: now 10V minimum for transmitter high level voltage
- Except for devices containing a bus power supply, the interface must be polarity insensitive
- Device marking requirements have changed
- Bus powered units are defined, allowing bus powered control gear and control devices
- Signal rise/fall times and signal timing improved and clarified
- 24-bit frames defined, and 20 & 32 bit frames reserved
- Multi-master timing defined
- Multiple logical units are now allowed within a single bus unit
- Part 101 now includes test sequences

Revision of Part 102: Control gear

- Fading rules/timing clarified
- Variable *lastActiveLevel* added. Command GO TO LAST ACTIVE LEVEL added
- Extended fade time for fades from 100 ms up to 16 minutes
- Operating modes allow manufacturer specific operation, and a standardised way to return to normal operation
- New WRITE MEMORY LOCATION - NO REPLY command, and RESET MEMORY BANK
- SAVE PERSISTENT VARIABLES command has been added
- QUERY LIGHT SOURCE TYPE added
- PING command defined, but to be ignored by control gear (allows detection of single masters)
- Physical selection has been removed
- Power-on and start-up timing has been updated and clarified
- Many additions and improvements to the test sequences (available to DiiA members)

2.2 Control device standardisation: Application controllers & input devices

Publication of Part 103 "*General requirements - Control devices"* also enabled publication of Parts 301-4, which specify the first four input device types. Input devices are a type of control device that provides information – an input – to the system. Another type of control device known as an *application controller* can use the information provided by input devices and other sources to allow them to make decisions and send commands to control gear.

Application controllers can operate as *single masters* or *multi-masters*. The bus communication requirements for both types are described in Part 103. Input devices are multi-masters, but are also capable of operating in a mode where they are simply polled by application controllers.

Highlights from Part 103 can be seen in the table below.

***New* Part 103: Control devices**
• Single masters and multi-masters allowed • *Input devices* defined • *Application controllers* defined • 24-bit frame format defined • Timing described in Part 101 • Addressing modes defined (64 short addresses, 32 group addresses, instance addressing, instance groups & feature type addressing) • *Events* defined • *Manufacturer specific modes* defined • Memory banks defined • Commands to enable and disable application controllers • *Quiescent mode* defined, where control devices shall not transmit any forward frames • *Event priorities* defined